Atty. Dkt. No. 029437-0108

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yasuhiro OKAMOTO et al.
Title:	FIELD-EFFECT TRANSISTOR HAVING GROUP III NITRIDE ELECTRODE STRUCTURE
Appl. No.:	10/538,739
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Examiner:	Sarah Kate Salerno
Art Unit:	2814
Confirmation Number:	7288

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.311, or an action that otherwise closes prosecution in the application.

RELEVANCE OF EACH DOCUMENT

The documents listed on the attached PTO/SB/08 were cited as being relevant during the prosecution of the corresponding Japanese application. A partial English translation of the Japanese Office Action of March 10, 2009, follows:

- Claim 8
- Reason 1
- Cited Literature 1–5
- Remarks

See Fig. 1 of Cited Literature 1, the description relating to Fig. 1, etc.

The invention described in Cited Literature 1 differs from the invention relating to Claim 8 in that the "surface passivation layer" (corresponding to the "insulation film" of Claim 8) is Si_3N_4 and is not an insulation film with a relative permittivity of 3.5 or less.

However, Cited Literature 2 describes an arrangement whereby the permittivity of the insulating film directly below the electrodes is lowered in a semiconductor element using a field plate structure for the electrodes, and states that this arrangement can resolve the technical problem that electric fields may become concentrated on the semiconductor element surface directly below the ends of the electrodes, leading to breakdown of the element (see page 1, right bottom column, line 1 to page 2, right top column, line 15; Figure 8, etc.).

Furthermore, it is obvious that the capacitance generated in the area directly below the electrodes can be reduced and that a semiconductor element with excellent high frequency gain can be obtained with this arrangement, and using an insulation film with a relative permittivity of 3.5 or less as the insulation film directly below an electrode is a commonly employed means (if necessary, see paragraphs (0026) and (0030) and Figure 22 (j) (BCB film 1408) of Cited Literature 3; paragraph (0026) and Figure 1 (air 19) of Cited Literature 4; paragraph (0027) and Figure 1 (fluorine resin 7) of Cited Literature 5; etc.).

Therefore, in the invention described in Cited Literature 1, making the insulation film into an insulation film with a relative permittivity of 3.5 or less instead of Si_3N_4 based on the descriptions in Cited Literatures 2 through 5 is a matter which could have been easily conceived of by a person skilled in the art.

• Claim 11

• Reason 1

• Cited Literature 1 and 6

• Remarks

See Fig. 1 of Cited Literature 1, the description relating to Fig. 1, etc.

The invention described in Cited Literature 1 differs from the inventions relating to Claim 11 in that it does not have an arrangement whereby the permittivity of the capacitance formed by the field plate part, the group III nitride semiconductor structure and the insulation film sandwiched between them is lower at the drain electrode side than at the gate electrode side.

However, Cited Literature 6 describes an arrangement whereby the capacitance formed by field plate part 9 and channel layer 2, and first dielectric film 4a and second dielectric film 4b sandwiched between them, gradually becomes smaller toward the drain electrode 8, and states that the technical problem of obtaining high withstand voltage characteristics by weakening the field relaxation effect due to the field plate part on the drain side to achieve an ideal electric field distribution can be resolved with this arrangement (see paragraphs (0057) through (0064), Figure 7, etc.).

In the invention described in Cited Literature 1 as well, this technical problem is obvious, and thus employing the arrangement described in Cited Literature 6 for the insulation film in the invention described in Cited Literature 1 is a matter which could have been easily conceived of by a person skilled in the art.

• Claims 13–15

• Reason 1

• Cited Literature 1–6

• Remarks

Regarding the specifying features of the inventions of Claims 13 through 15, see "undoped $Al_{0.3}Ga_{0.7}N$" of Cited Literature 1 (corresponding to the "contact layer" of Claims 13 through 15").

• Claim 16

• Reason 1

• Cited Literature 1–7

• Remarks

Regarding the specifying features of the inventions of Claim 16, see "GaN buffer layer" (corresponding to the "channel layer consisting of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$)" of Claim 16), "$Al_{0.3}Ga_{0.7}N$" (corresponding to the "electron source layer consisting of $Al_yGa_{1-y}N$ ($0 \leq y \leq 1$)" of Claim 16) and "GaN cap layer" (corresponding to the "cap layer comprising GaN" of Claim 16) of Cited Literature 7.

<Claims for which no reasons for rejection have been discovered>

No reasons for rejection have been discovered as of now for the inventions relating to claims (1 through 7, 9, 10 and 12). If any reasons for rejection are newly discovered, a notification of reasons for rejection will be issued.

List of Cited Literature

1. J. Li, et al., High breakdown voltage GaN HFET with field plate, Electronics letters, U.K., IEE, February 1, 2001, Vol. 37, No. 3 pp. 196–197

2. Japanese Unexamined Patent Application Publication H02–072667

3. Japanese Unexamined Patent Application Publication 2000–353708

4. Japanese Unexamined Patent Application Publication H09–027505

5. Japanese Unexamined Patent Application Publication H08–083813

6. Japanese Unexamined Patent Application Publication 2001–230263

7. Shawn T. Bradley et al., Influence of AlGaN Deep Level Defects on AlGaN/GaN 2-DEG Carrier Confinement, IEEE transactions on electron devices, U.S.A., IEEE, March 2001, Vol. 48, No. 3, pp. 412–415

(Note) Some or all of the presented non-patent literature may not be mailed in some cases due to legal, contractual or other restrictions.

A copy of Document C7 is not attached, as this document was provided with Applicants' information Disclosure Statement submitted on March 11, 2008.

Any document listed on the attached PTO/SB/08 was cited as being relevant during the prosecution of the corresponding Japanese application. A copy of the Japanese Search Report is attached setting forth the portion of each document considered relevant by the examiner. An English-language counterpart of the foreign-language documents has not been provided. The absence of a translation or an English-language counterpart document does not relieve the PTO from its duty to consider any submitted document (37 CFR §1.98 and MPEP§609).

Applicants respectfully request that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

STATEMENT

The undersigned hereby states in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to filing of this Statement.

The undersigned hereby states in accordance with 37 CFR §1.704(d) that each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 CFR §1.56(c) more than thirty days prior to the filing of the information disclosure statement.

Although Applicant believes that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

Reg. No. 38,819

Date: April 6, 2009

By Phillip J. Articola

for /

George C. Beck
Attorney for Applicant
Registration No. 38,072

FOLEY & LARDNER LLP
Customer Number: 22428
Telephone: (202) 945-6014
Facsimile: (202) 672-5399